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PATENT APPLICATION



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sinclair et al.
Serial No. 09/325,882
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Examiner: Harold Kim
Art Group: 2182
Our file no. 00100.99.0039
Docket No. 0100.9900390

**Title: POWER REDUCTION CIRCUIT AND METHOD WITH MULTI CLOCK
BRANCH CONTROL**

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Attn: Examiner Harold Kim

9/12/02
Date:

Rosalie Swanson
Rosalie Swanson

PRELIMINARY AMENDMENT

Dear Sir:

Applicants respectfully submit the following Preliminary Amendment to be entered with the Request for Continued Examination.

In the claims:

✓
Please amend Claims 1, 7, 8, 12, 13 and 16 as follows. In particular, please substitute the below claims for the indicated pending claims with the same number. Please add new Claims 17, 18 and 19.

- Sub C7
BT
1. (Twice Amended) A power consumption reduction circuit comprising:
a memory clock source for a graphics controller; and
a memory clock tree circuit, operatively coupled to the memory clock source, that generates branches of memory clock output signals as a plurality of corresponding independent clock signals to a number of memory interface circuits for differing processing engines and